**Massachusetts Institute of Technology**
**Department of Electrical Engineering and Computer Science**

# 6.002 – Circuits & Electronics
**Fall 2018**

# Quiz #2

**14 November 2018**

**Name:** ______________________________

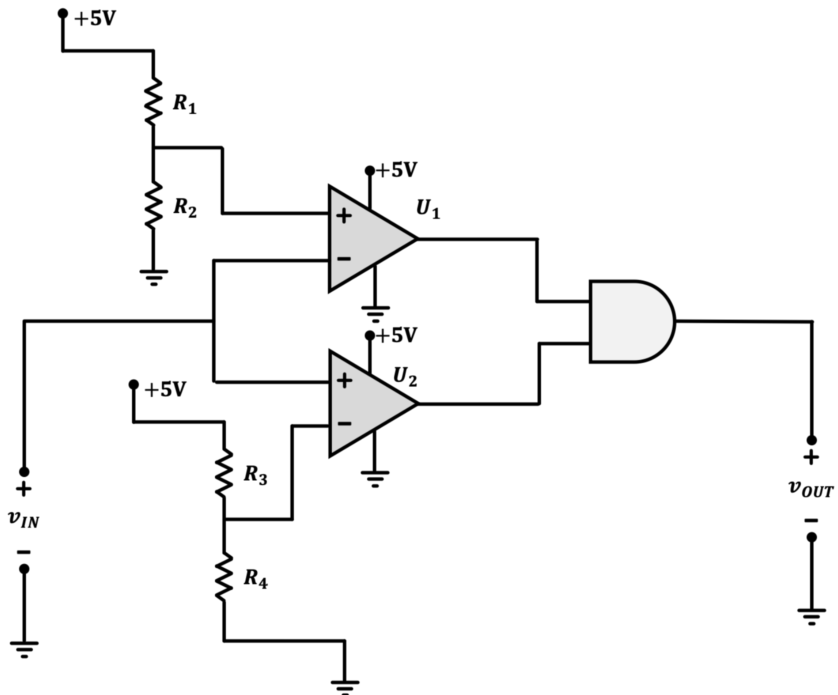
**Recitation Time:** 11 12 1

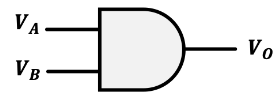
- There are 19 pages in this quiz, including this cover page.
- Please put your name in the space provided above, and circle the time of your recitation.
- Please do not remove any pages from this quiz.
- Do your work for each question within the boundaries of that question, or on the back of the preceding page. *When finished with each part, clearly write your answer for that part into the corresponding answer box or graph.*
- *All numerical answers require proper units.*
- *All answers must be justified by supporting math and/or explanations in order to receive full credit.*
- This is a closed-book quiz, but calculators and a single two-sided page of notes are allowed.
- Good luck!

| **Problem 1** | **Problem 2** | **Problem 3** |
|---|---|---|
| | | |
| **Problem 4** | **Problem 5** | **Total Grade** |
| | | |

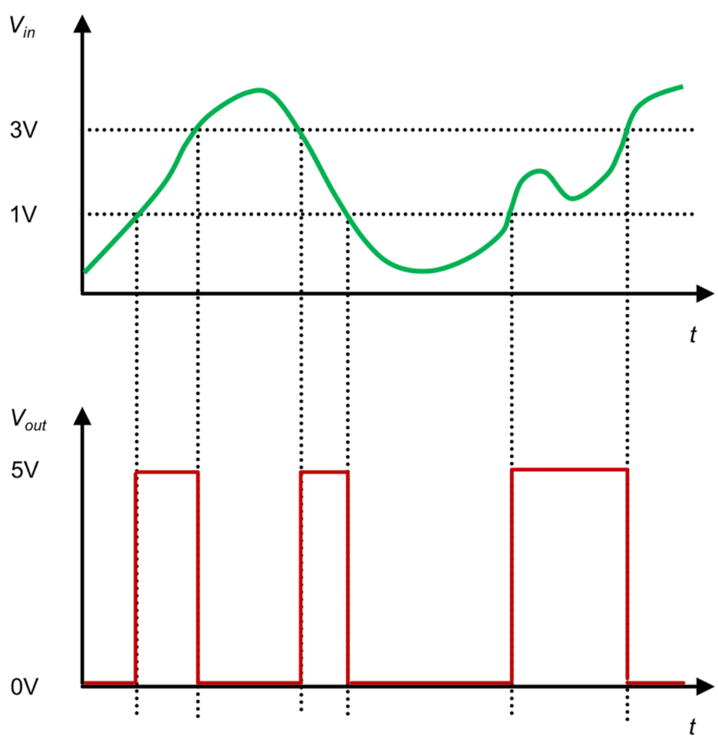
### Problem 1: Comparators & Windows – 15%

The circuit shown below utilizes the two comparators U1 and U2 (without positive feedback), a logical AND gate, and four resistors to implement a window comparator. The truth table for the logical AND gate, and an input-output relation for the window comparator over time, are also shown below.



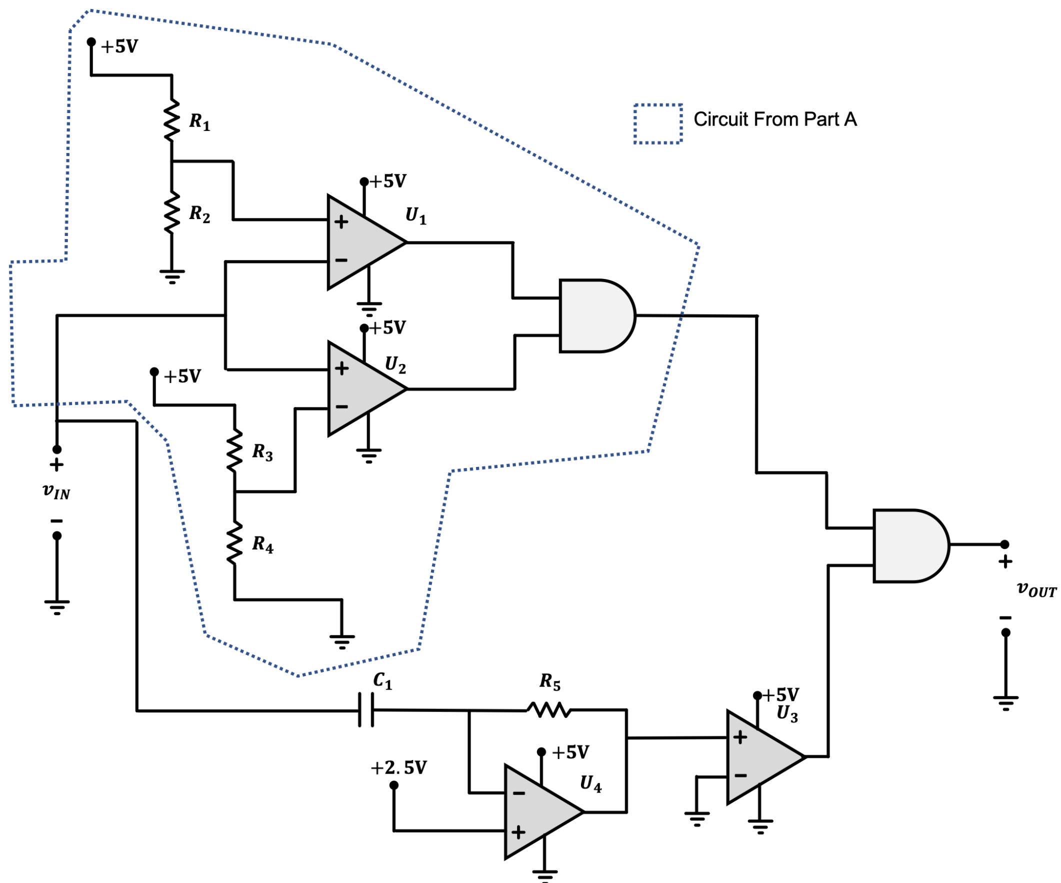

| $V_A$ | $V_B$ | $V_O$ |
|---|---|---|
| 0V | 0V | 0V |
| 0V | 5V | 0V |
| 5V | 0V | 0V |
| 5V | 5V | 5V |

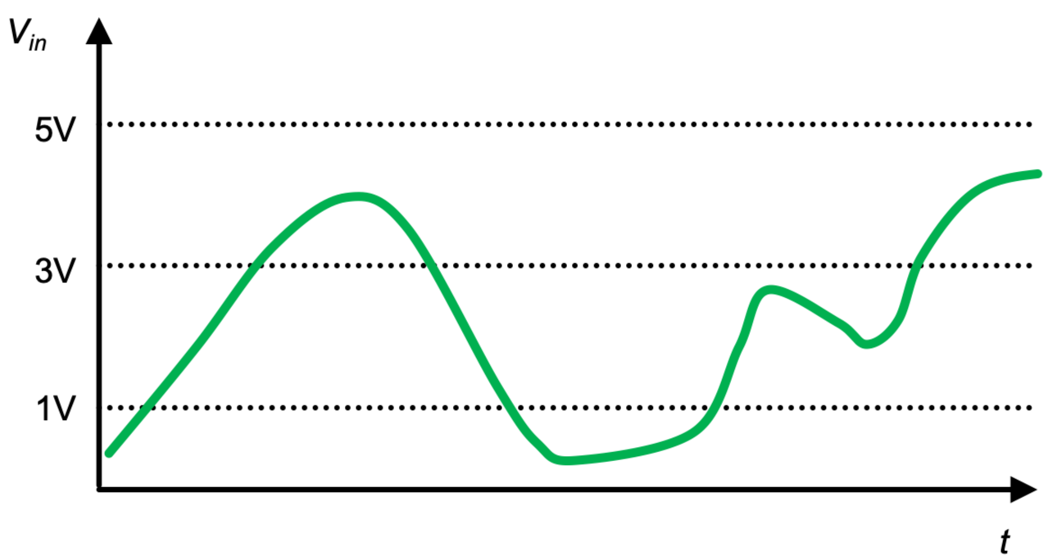


(1A) Determine numerical values for resistors $R_1$ $R_2$, $R_3$ and $R_4$ so as to achieve the input-output relation of the window comparator shown above. In doing so, let the resistance range for all resistors be $1\ \text{k}\Omega \le R \le 10\ \text{k}\Omega$.

| $R_1$ | $R_2$ | $R_3$ | $R_4$ |
|---|---|---|---|
| | | | |

(1B) The window comparator from Part (A) is augmented with the addition of an operational amplifier, a comparator, a resistor, a capacitor and a logical AND gate as shown below. Assume that operational amplifier U4 is ideal; U1, U2 and U3 are comparators. Also shown below is a section of $v_{\mathrm{IN}}(t)$. Determine the corresponding $v_{\mathrm{OUT}}(t)$ and graph it on top of the $v_{\mathrm{IN}}(t)$ shown below. Additionally, briefly explain the operation of the augmented window comparator on the next page.



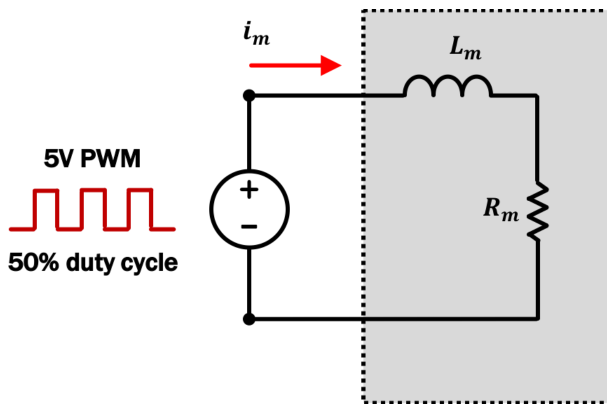



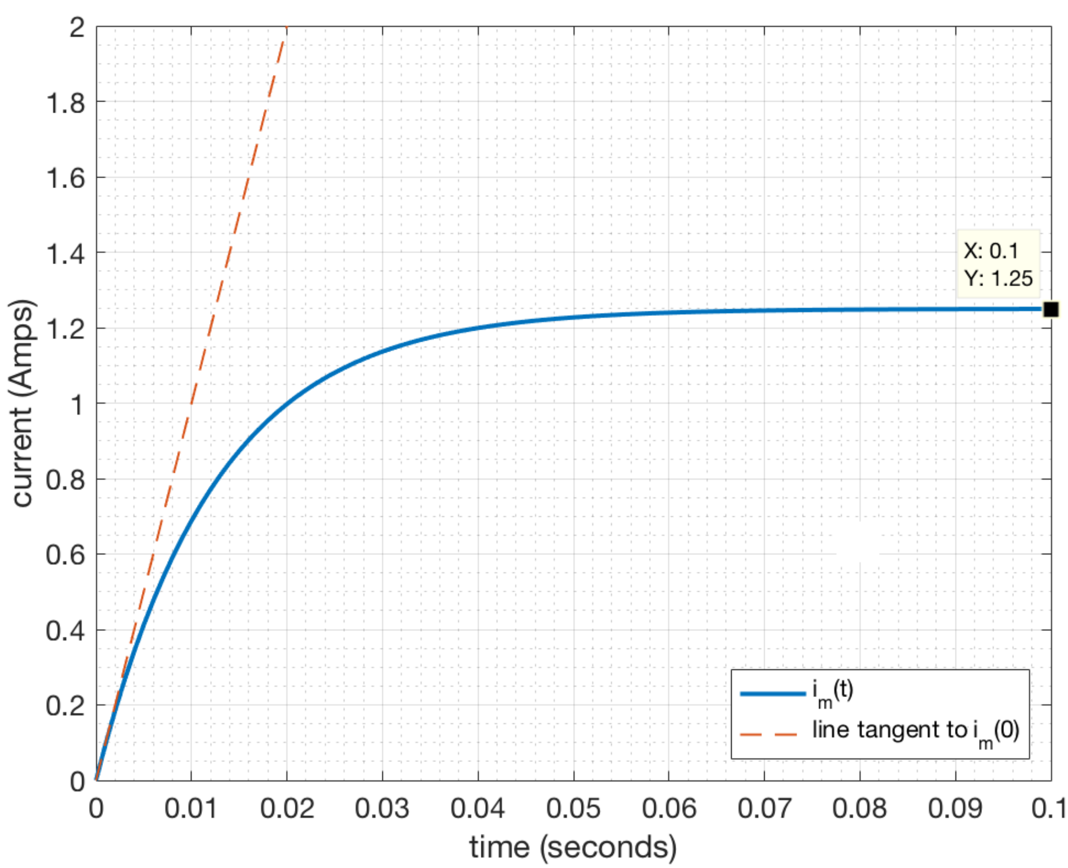
Briefly explain the operation of the window comparator here.

**Problem 2: Pulse Width Modulation – 30%**

This problem involves networks driven by a square wave that alternates between 0 V and 5 V with a 50% duty cycle.

(2A) A first-order resistor-inductor network is driven by the square wave as shown below. Assume for this part that the half-period of the square wave is long enough that the network reaches a steady state after both input switching transitions. A corresponding measurement of the current $i_m$, starting at the time of the rising edge of the 5-V square wave, is shown below. Here $t = 0$ is defined as the time at which the input voltage transitions from 0 V to 5 V. Using the measured data, numerically determine $R_m$ and $L_m$.



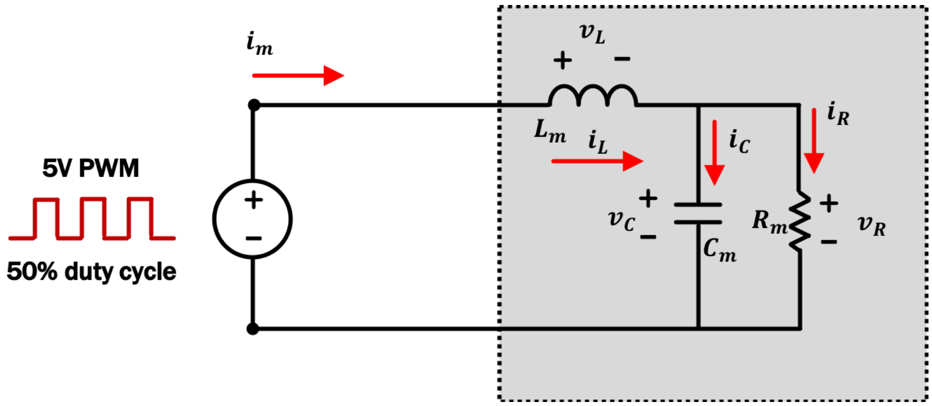



| $R_m$ | $L_m$ |
|---|---|
| | |

(2B) Let the square-wave period be reduced to 40 ms while the duty cycle remains at 50%. For this case, numerically determine the average value of the current $i_m$ in the cyclic steady state.

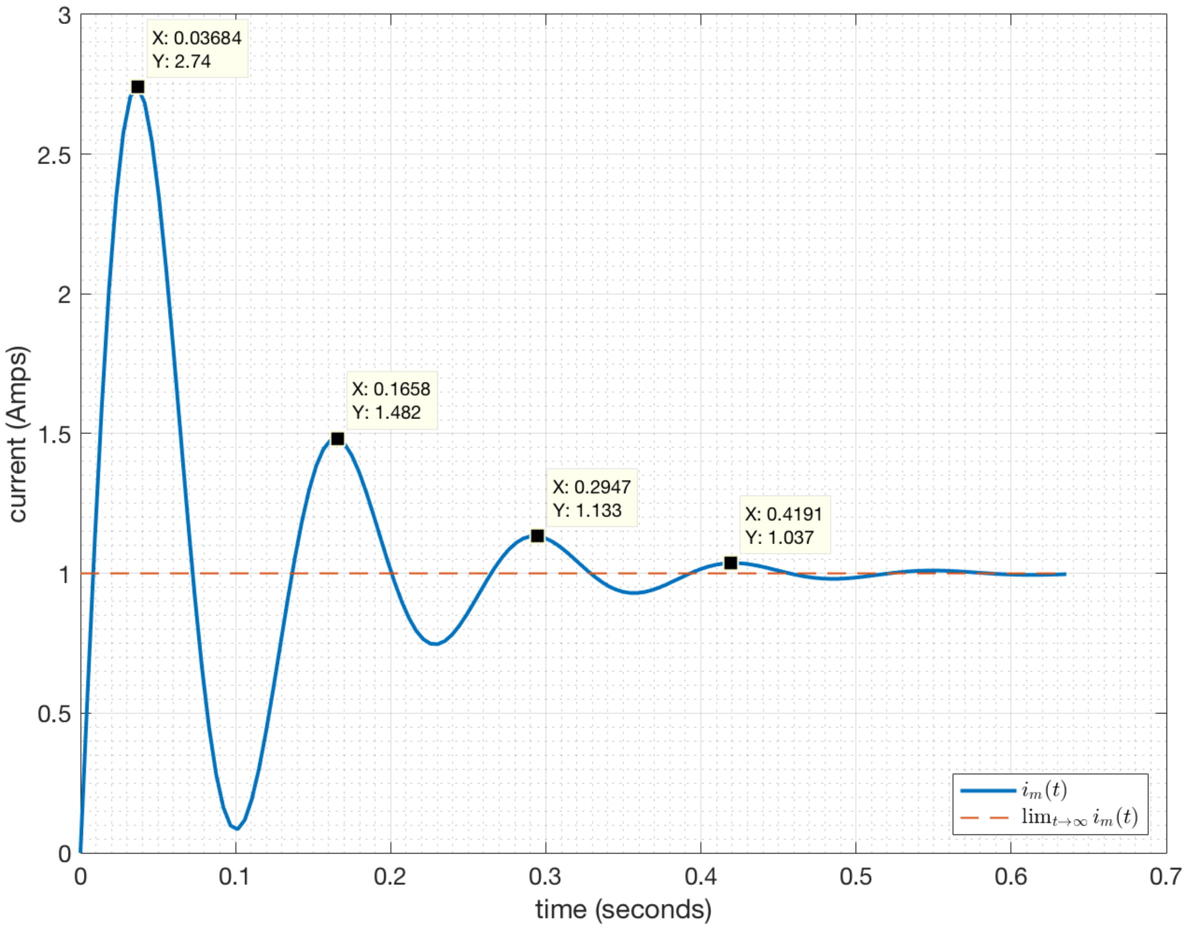
| Average $i_m$ |
| --- |
| |

(2C) A capacitor is added to the circuit of Parts (A) and (B) resulting in the similar but higher-order circuit shown below. Assuming that the half-period of the input square wave is long enough to allow all transients to settle, determine the following branch variables long after the input voltage has switched to 5 V. *Provide answers in terms of $R_m$, $L_m$, $C_m$, and the square wave parameters.*




| $v_R$ | $v_L$ | $v_C$ |
|---|---|---|
| | | |
| $i_R$ | $i_L$ | $i_C$ |
| | | |

(2D) A corresponding measurement of the current $i_m$, starting at the time of the rising edge of the 5-V square wave, is shown below. Here $t = 0$ is again defined as the time at which the input voltage transitions from 0 V to 5 V. Using the measured data, numerically determine $R_m$, $L_m$ and $C_m$. In doing so, again assume that the half-period of the square wave is long enough that the network reaches a steady state after both input switching transitions.



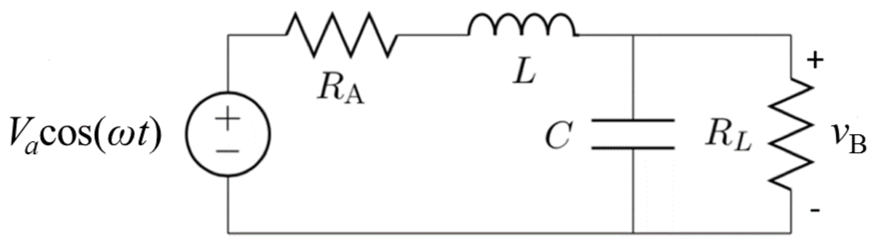

| $R_{\mathrm{m}}$ | $L_{\mathrm{m}}$ | $C_{\mathrm{m}}$ |
|---|---|---|
| | | |

(2E) The oscillatory response of the circuit is deemed to be undesirable. It is instead required to remove all overshoot in the current while still allowing the circuit to "settle" at the rate achieved in Part (2D). It is also required that current $i_m$ settles to the same value as in the transient in Part (2D). In order to meet these requirements with the same 5-V input, should $R_m$, $L_m$ and $C_m$ each be increased decreased, or left unchanged? Circle the correct answers.

| $R_{\mathrm{m}}$ | $L_{\mathrm{m}}$ | $C_{\mathrm{m}}$ |
|---|---|---|
| Increase | Increase | Increase |
| Decrease | Decrease | Decrease |
| Unchanged | Unchanged | Unchanged |

**Problem 3: Holiday Lights – 20%**

Our holiday-light lab involved designing a resonant circuit to maximize an output voltage used to power a string of light-emitting diodes (LEDs). This problem considers a more realistic situation in which the circuit includes the output resistance of the driving signal generator, and the parasitic resistance of the inductor. The circuit, which operates in the sinusoidal steady state, is shown below. In this circuit, $R_{\mathrm{A}}$ is the series sum of the Thevenin resistance of the signal generator and the inductor parasitic resistance, and $R_{\mathrm{L}}$ is a linear load resistance that models the (nonlinear) LEDs.




(3A) Determine the transfer function $\tilde{V}_{\mathrm{b}}(j\omega)/V_{\mathrm{a}}$.

| Transfer Function |
| --- |
| |

(3B) Express the quality factor Q of this circuit as a function of $R_{\mathrm{A}}$, $R_{\mathrm{L}}$, C and L. Hint: the quality factor is defined as $\omega_0/2\alpha$, where $\omega_0$ and $\alpha$ are the undamped resonant frequency and the damping of the circuit, respectively.

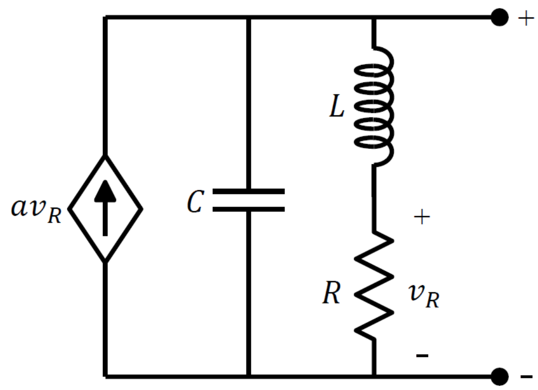
| $Q$ |
| --- |
| |

(3C) Let $L = 50$ mH, $C = 10$ nF, $R_{\text{A}} = 100\ \Omega$, $R_{\text{L}} = 50\ \text{k}\Omega$, and $V_{\text{A}} = 3.3$ V. In this case, what is the maximum number of holiday lights that can be lit up if each LED requires 2.4 V? What numerical frequency $\omega$ should be used to achieve this maximum?

| Maximum Number | Frequency $\omega$ |
| --- | --- |
| | |

**Problem 4: Sinusoidal-Steady-State Thevenin Equivalence – 20%**

This problem concerns the linear network shown below operating in the sinusoidal steady state.




(4A) Determine the Thevenin equivalent network looking into the port given that $a = 0$.

| $\tilde{V}_{\text{th}}$ | $Z_{\text{TH}}$ |
|---|---|
| | |

(4B) Determine the Norton equivalent network looking into the port given that $a = 0$.

| $\tilde{I}_{\mathrm{n}}$ | $Z_{\mathrm{N}}$ |
|---|---|
| | |

(4C) Determine the Thevenin equivalent network looking into the port given that $a = \frac{1}{2}$ [S].

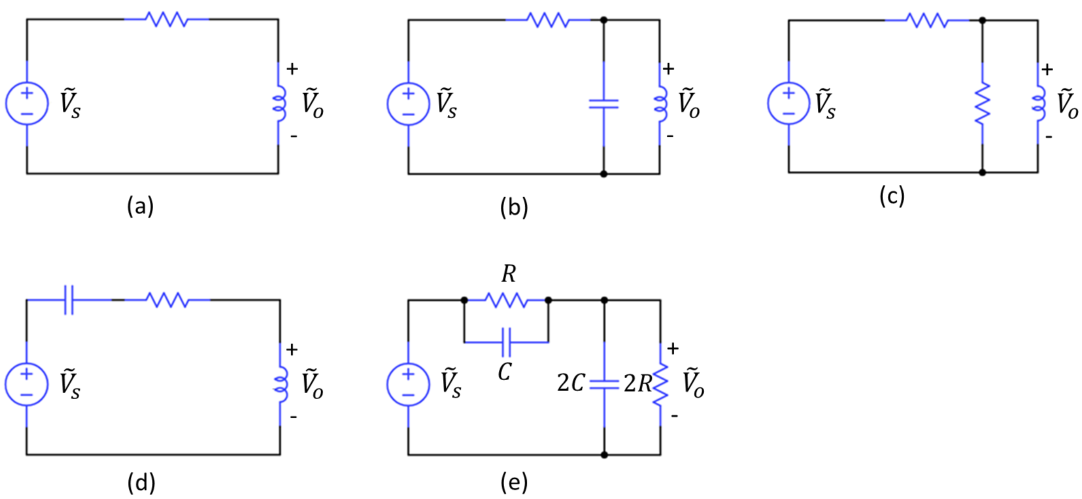
| $\tilde{V}_{\text{th}}$ | $Z_{\text{TH}}$ |
|---|---|
| | |

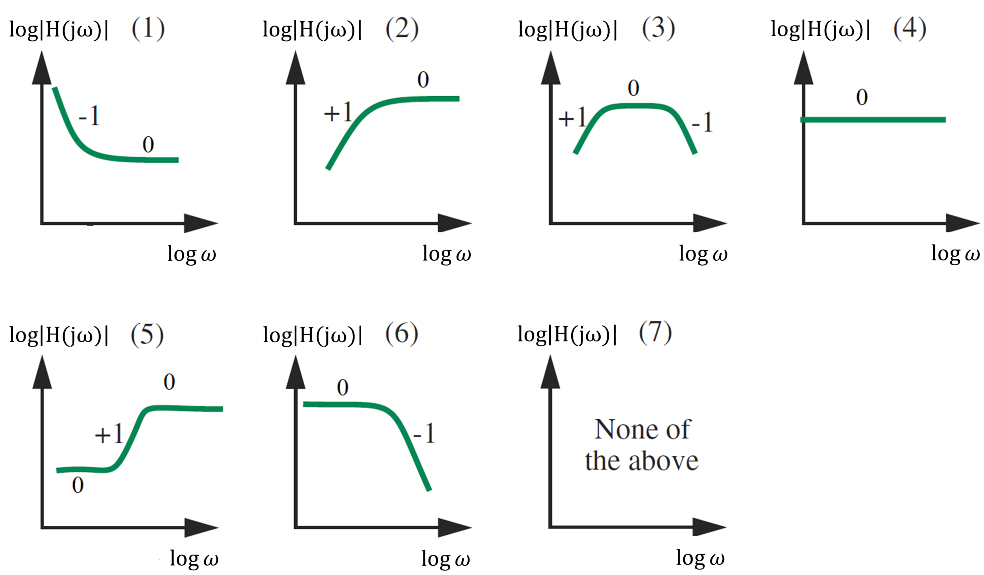
(4D) Determine the Norton equivalent network looking into the port given that $a = \frac{1}{2}$ [S].

| $\tilde{I}_{\mathrm{n}}$ | $Z_{\mathrm{N}}$ |
|---|---|
| | |

**Problem 5: Sinusoidal-Steady-State Transfer Functions – 15%**

Five circuits are shown below together with eight magnitude plots. The magnitude plots show possible input-output transfer function magnitudes, namely $|\tilde{V}_o/\tilde{V}_s|$ as functions of the frequency $\omega$. Note that both the frequency and magnitude axes are drawn with a log scale, and that the numbers -1, 0, and +1 denote the local slope of the transfer functions in decades per decade. For each circuit, (a) through (e), determine the corresponding magnitude plot (1) through (7). Note that one magnitude plot might correspond to more than one circuit.




| Circuit | (a) | (b) | (c) | (d) | (e) |
|---|---|---|---|---|---|
| Magnitude Plot | | | | | |